Physical Aspects of Negative Oxide Charge in p-MOS Capacitors with Annealed ITO Gates

Oleksandr Malik, F. Javier De la Hidalga-Wade

***Abstract*— Properties of p-MOS capacitors with tin-doped indium oxide (ITO) gates have been investigated. The use of a transparent conducting gate is important for applications of p-MOS capacitors as optical sensors. A significant shift of the capacitance-voltage characteristics was observed, and this is explained as due to the presence of a negative oxide charge at the ITO-silicon dioxide interface. This negative charge comes from the presence of indium atoms that have diffused into the silicon dioxide**

***Index Terms*—p-MOS capacitor, silicon. tin-doped indium oxide, oxide charge.**

I. Introduction

Metal-oxide-semiconductor (MOS) capacitors with a semi-transparent poly-silicon gate are widely used as optical sensing elements in charge coupled silicon devices (CCDs). An inherent advantage of MOS sensors in comparison with diodes can be achieved when the gate is fully transparent. Tin-doped indium oxide thin films usually are used as transparent conducting gate in high sensitive CCDs. The main feature of this material is the perfect combination of electrical conductivity and optical transparency. We reported other applications of MOS capacitors as optical sensors with a direct pulse-width modulated (PWM) electrical output [1,2]. These devices are based on p-MOS capacitors fabricated on n-type silicon substrates. The duty of the PWM output depends on the light intensity. These capacitors operate in non-equilibrium depletion mode biased with a saw tooth-like applied voltage. For their successful operation, and taking into account a positive fixed charge at the silicon dioxide-silicon interface, which leads to a high negative value of the threshold voltage, the capacitors need to be biased in inversion by applying a constant negative voltage. The need of two voltage sources is a drawback of these devices. Moreover, the reported devices were fabricated with non-transparent aluminium gates, thus only the perimeter edge and a small area within a diffusion length of minority carriers can be illuminated by photons. The use of a transparent conducting ITO gate allows for a homogeneous illumination on the whole area of the MOS capacitor.

It has been observed [3] that the annealing of ITO-SiO_2-Si capacitors, in oxygen atmosphere at temperatures above 400^{o}C leads to a considerable shift of the capacitor-voltage (C-V) characteristics. This has been explained as a possible change of the work function of the ITO films due to the chemical absorption of oxygen atoms on the surface of the ITO grains.

In this work we discuss a different and more accurate physical aspects to explain this significant shift on the C-V characteristics.

II. Fabrication

MOS capacitors were fabricated on n-type 3-5 Ω-cm silicon wafer. The SiO_2 layer, with a thickness around 70 nm, was grown at 1000^{o}C. Then, the wafer was cut in two parts for the fabrication of capacitors with Al and ITO gates. An aluminum layer was deposited at the back of both SiO_2-Si structures and on the SiO_2 film of the wafer part for Al gate, followed by a post-annealing in forming gas for electrical contact. On the other part of the wafer, the ITO layer was deposited over the SiO_2 film by DC magnetron sputtering in pure argon atmosphere at 100 W of power under a 3 mTorr working pressure.

A photolithography process was applied for etching the Al and ITO layers to obtain the MOS capacitors with a gate area of 2x3 mm^2. The capacitors with ITO gates were divided in several parts for annealing in the oxygen atmosphere at different temperatures for 1 hour.

III. Results

As-deposited, the ITO films presented a low conductivity and transparency. Considerable improvement of the film properties was observed after annealing in the oxygen atmosphere. The obtaining of poor properties of as-deposited ITO films is connected with the composition of the sputtered target, the black colour of which testifies the presence of foreign phases as metallic tin, indium and/or blue/black sub-oxides of tin and indium connected with the reducing atmosphere used in the fabrication method [3]. Annealing in an oxygen atmosphere allows for obtaining transparent stoichiometric ITO films, whose conductivity is determined by the tin atoms as well as by the presence of oxygen vacancies. The sheet resistance of the annealed ITO films is shown in Fig. 1.

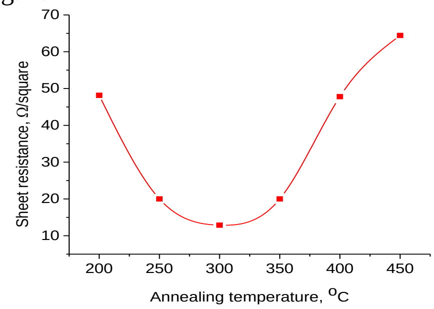

Fig. 1 Sheet resistance of the 200 nm thick ITO film deposited on the SiO_2 layer after annealing in the oxygen atmosphere at different temperatures.

Oleksandr Malik, Instituto Nacional de Astrofísica, Óptica y Electrónica (INAOE), Electronics Department, PO Box 51 and 216, Puebla, Mexico, +522222470517

F. Javier De la Hidalga-Wade, Instituto Nacional de Astrofísica, Óptica y Electrónica (INAOE), Electronics Department, PO Box 51 and 216, Puebla, Mexico, +522222470517

The minimum of the sheet resistance is due to a high concentration of electrons coming from the joint action of the activated tin ions and the oxygen vacancies which are donors in In_2O_3. The increase of the sheet resistance at annealing temperatures above 300°C is due to the reduction of the oxygen vacancies. The transmittance of the ITO films deposited on a glass substrate and annealed at different temperatures is shown in Figure 2.

The carrier concentration, determined by Hall measurements for the ITO films annealed at 300°C is 10^{21} cm^{-3}. The films annealed at the temperature range of 400-500°C presented a lower carrier concentration (1.5×10^{20} cm^{-3}) due to the decrease of oxygen vacancies.

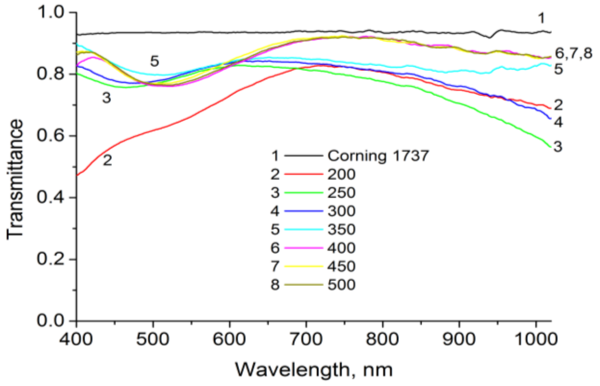

Fig. 2 Transmittance of the ITO films deposited on Corning 1737 glass substrate and annealed at different temperatures.

Low frequency C-V characteristics of the ITO-SiO_2-Si capacitors with the ITO film annealed in the oxygen atmosphere at different temperatures are compared to the characteristic of the Al-SiO_2-Si capacitor in Fig. 3. Capacitors with Al gate, as well as with ITO gate annealed at 300°C and 350°C, present nearly the same C-V characteristics with a threshold voltage around -1V. The threshold voltage of the capacitors with the ITO gate annealed at 400°C and 450°C is significantly different, -0.6V and 0.25 V, respectively. Initially, one can think that the significant shift of the C-V characteristics could be explained by a significant difference of the work functions of the ITO films annealed at 400°C and 450°C in comparison with the films annealed at lower temperatures. Such hypothesis needs a more detailed discussion.

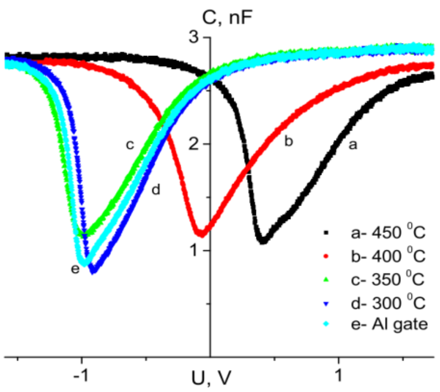

Fig. 3 C-V characteristics of the ITO-SiO_2-Si capacitors with ITO films annealed in the oxygen atmosphere at different temperatures. The C-V characteristic of Al-SiO_2-Si capacitor is also shown.

IV. Discussion

The increase of the ITO work function at high annealing temperatures cannot be explained as due to the shift of the Fermi level in highly degenerated ITO films; this is because there is a small difference (less than one order of magnitude) in carrier concentrations between the films annealed at low and high temperatures. The calculated value of such shift is close to 0.5V, if the reduced effective mass of electrons in the ITO films is supposed to be 0.5 m_0 [4].On the other hand, the increase of the work function for the ITO films annealed at high temperature could be explained considering the oxygen atoms adsorbed on the grain boundary inside the ITO films. At low temperatures this adsorption is physical, whereas at high temperatures a chemical adsorption takes place [5]; namely, at temperatures above 350°C, the oxygen molecule adsorbed on the film grains dissociates into oxygen atoms, each one of them takes one conduction electron from the ITO to form oxygen ions, thus the oxygen is bound with the grains by electrons. The presence of negatively charged oxygen ions produces a band-bending at the grain's surface. In non-degenerated semiconductors with moderate carrier concentration such superficial band-bending can increase the work function. However, in the ITO films with carrier concentration around 10^{20} cm^{-3} the width of the potential barrier is nearly 2 nm. The carriers can easily overcome this barrier by tunneling and the work function would not undergo considerable changes.

At this stage we would like to draw attention to a model of appearance of negative charge at the ITO/SiO_2 interface. At temperatures above 350°C indium atoms can diffuse into the silicon oxide coming from a non-stoichiometric amorphous as-deposited ITO film during the annealing process. Thus, if trivalent indium atoms replace tetravalent silicon atoms in the elementary Si_4O_8 tetrahedron, a negative charged $(InSi_3O_8)^{-1}$ network can be formed. In the case that two indium atoms occupy the position of silicon atoms in the tetrahedron, a double charged negative $(In_2Si_3O_8)^{-2}$ network may be formed. A fixed negative charge at the ITO/SiO_2 interface can balance a positive charge at the SiO_2-Si interface; this can explain the considerable shift observed in the C-V characteristics in capacitors with ITO gates annealed at high temperatures. Since the indium diffusion coefficient increases with temperature, the shift of the C-V characteristic must be higher for capacitors with ITO gates annealed at 450°C.

It is worth mentioning that the diffusion of indium atoms from the ITO film though SiO_2 has already been reported for organic light emitting diodes reported in [6,7].

Using well known equations for p-MOS capacitors [8], the negative charge necessary for obtaining a zero threshold voltage (V_t) for capacitors fabricated on silicon substrates with different donor concentrations, was calculated assuming values of 10^{10} cm^{-2} and 5×10^{10} cm^{-2} for the fixed positive charge presents at the SiO_2/Si interface. The work function of the ITO films was assumed as 4.6 eV, and the results are shown in Fig- 4.

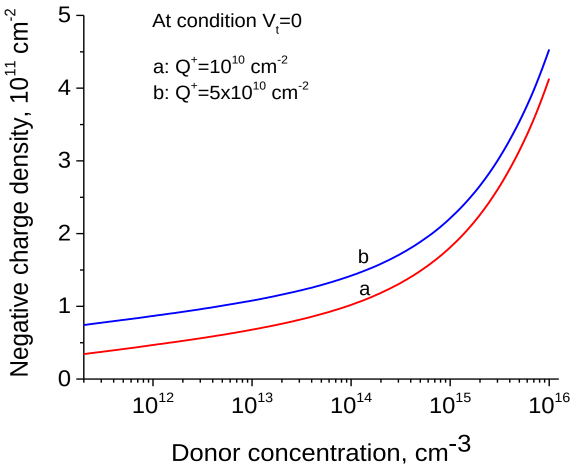

Fig. 4 Calculated value of the negative charge necessary to obtain a zero threshold voltage in p-MOS capacitors fabricated on silicon substrates with different donor concentration.

From Fig. 4 the value of the negative charge necessary to satisfy the condition V_t=0 V for our used silicon substrates is in the $(1\text{-}2)\times10^{11}$ cm^{-2} range. For capacitors with the ITO film annealed at 450°C, the threshold voltage is 0.25 V, which makes clear the higher value of negative charge necessary for overcompensation of the fixed positive charge at the SiO_2-Si interface.

Experimental evidence of metal-induced negative charge in silicon dioxide grown on n-type silicon wafers, which were previously rinsed with an RCA alkaline solution contaminated with trivalent aluminum or iron, were reported in [9-11]. The authors analyzed the frequency-dependent AC surface photovoltage, and showed that the negative charge density in naturally or thermally SiO_2 films grown on contaminated silicon wafers can exceed the value of 10^{11} cm^{-2}. It was suggested that the negative induced charge is the result of the formation of $(AlSiO)^{-1}$ or $(FeSiO)^{-1}$ networks (note, that the reported chemical formulas do not correspond to the elements valences) occurring when Al or Fe atoms substitute silicon atoms in the SiO_2 layer. Since indium is an element of the same column of the periodic table as Al, the formation of similar negative networks can take place.

V. Conclusion

Based on our research, it is shown that p-MOS capacitors on n-type silicon substrates with ITO gates deposited by DC sputtering technique in pure argon atmosphere and annealed in oxygen at a temperature above 400°C present a zero or positive value of the threshold voltage. Such capacitors, working as novel optical sensors with direct PWM output signal, and operating without a constant voltage, were fabricated and their properties will be discussed in a future publication.

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Oleksandr Malik, PhD, Titular Researcher, Electronics Department, Instituto Nacional de Astrofísica, Óptica y Electrónica (INAOE), Electronics Department, Puebla, Mexico.

F. Javier De la Hidalga-Wade, PhD, Titular Researcher, Electronics Department, Instituto Nacional de Astrofísica, Óptica y Electrónica (INAOE), Electronics Department, Puebla, Mexico.